REMARKS

Claims 1-50 are currently pending in the application. This amendment is in response to the Office Action of May 17, 2001.

Claim Objections-Lack of Antecedent Basis

Claims 1,8, 26, and 33 were objected to because there is no antecedent basis in the claims for "the board." Appropriate corrections have been made.

35 U.S.C. § 112 Rejections

Claims 17, 20, 42, and 45 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended the claimed invention as suggested by the Examiner for the presently claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 17, 20, 42, and 45 are allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 103(a) Obviousness Rejections

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants request reconsideration of the application in view of the arguments set forth below.

Applicants further submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination

and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure. See M.P.E.P. 706(j).

Obviousness Rejection Based on U.S. Patent No. 5,674,785 to Akram in view of U.S. Patent No. 5,293,068 to Kohno

Claims 1-16, and 26-41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram et al. (U.S. Patent No. 5,674,785) in view of Kohno et al. (U.S. Patent No. 5,293,068).

Applicant, respectfully, submits that the prior art references individually or in combination do not teach or suggest the claim limitation of bond pads on the second attachment surface of a substrate which is present in independent claims 1, 5, 8, 12, 26, 30, 33, and 37. Examiner relies on the combination of Akram and Kohno to teach all of the elements of these independent claims. In the rejection it is stated that Kohno discloses in FIG. 4 bond pads on a second attachment surface of a substrate (2). Kohno is relied on to teach this element since it is not taught or suggested by Akram. However, Applicant submits that Fig. 4 of Kohno does not disclose bond pads. FIG. 4, which is a cross section of FIG. 3 discloses a conducting pattern 4. As shown in FIG.3, conducting pattern 4 are not bond pads but are long conducting elements. Therefore, it is improper to rely on Kohno to teach this part of Applicant's claims. The prior art references individually or in combination do not teach or suggest the claim limitation that bond pads on the second attachment surface of a substrate found in independent claims 1, 5, 8, 12, 26, 30, 33, and 37. Independent claims 1, 5, 8, 12, 26, 30, 33, and 37 are allowable for the reasons stated above. Further dependent claims 2-4, 6 and 7, 9-11, 13-16, 27-29, 31 and 32, 34-36, and 38-41 are allowable since they depend on nonobvious independent claims.

Obviousness Rejection Based on U.S. Patent No. 6,013,948 to Akram$_1$ in view of U.S. Patent No. 5,293,068 to Kohno

Claims 17, 19, 42, and 44 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram$_1$ et al. (U.S. Patent No. 6,013,948) in view of Kohno et al. (U.S. Patent No. 5,293,068). Applicant will not address the merits of this rejection since Akram$_1$ cannot be used as a prior art reference. This application claims priority, as stated in the first full paragraph of the specification, to U.S. Patent 5,719,440, issued February 17, 1998 filed December 19, 1995. The effective filing date of Applicant's application (December 19, 1995) is prior to Akram$_1$ filing date of April 1, 1998. Applicant submits that the rejection based on Akram$_1$ should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 6,013,948 to Akram$_1$ in view of U.S. Patent No. 5,293,068 to Kohno and further in view of U.S. Patent No. 5,674,785 to Akram

Claims 18 and 43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram$_1$ et al. (U.S. Patent No. 6,013,948) in view of Kohno et al. (U.S. Patent No. 5,293,068). For the reasons stated above Akram$_1$ cannot be used as a prior art reference and the rejection should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,674,785 to Akram in view of U.S. Patent No. 5,293,068 to Kohno and U.S. Patent No. 6,013,948 to Akram$_1$

Claims 20-25, and 45-50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akram et al. (U.S. Patent No. 5,674,785), in view of Akram$_1$ et al. (U.S. Patent No. 6,013,948) and Kohno et al. (U.S. Patent No. 5,293,068). For the reasons stated above Akram$_1$ cannot be used as a prior art reference and the rejection should be withdrawn.

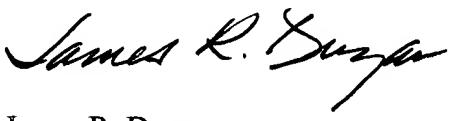
ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 8, 17, 20, 26, 33, 42, and 45 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1-50 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Date: August 2, 2001
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace the first full paragraph on page 2 with the following:

This application is a divisional of application Serial No. 09/483,483, filed January 14, 2000, pending, which is a continuation of application Serial No. 08/948,936, filed October 10, 1997, [pending] now U.S. Patent 6,201,304 B1, issued March 13, 2001, which is a continuation of application Serial No. 08/574,662, filed December 19, 1995, now U.S. Patent 5,719,440, issued February 17, 1998.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Amended) A method of electrically connecting a semiconductor die to a substrate, comprising:

providing a semiconductor die having a surface having a plurality of bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the [board] substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the [board] substrate;

attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said [board] substrate; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said [board] substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said [board] substrate.

8. (Amended) A method of electrically connecting at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die having a surface having a plurality of bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the [board] substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the [board] substrate;

attaching the surface having a plurality of bond pads thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the [board] substrate having the plurality

of bond pads of the semiconductor die located over one of the at least two vias extending through the [board] substrate ; and

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads of said [board] substrate using a plurality of wire bonds, said plurality of wire bonds extending through the one via extending through the board of the at least two vias extending through the [board] substrate.

17. (Amended) A method of electrically connecting a semiconductor die to a master board, comprising:

providing a semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the die side surface of the board to the circuit traces of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds[, said plurality of wire bonds extending through the at least one via extending through then board]; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

20. (Amended) A method of electrically connecting a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting [the] a plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds[, said plurality of wire bonds extending through the a via extending through then board]; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.

26. (Amended) A method of attaching a semiconductor die to a substrate, comprising:

providing a semiconductor die having a surface having at least one bond pads thereon;

providing a substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the [board] substrate;

attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said [board] substrate; and

connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said [board] substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said [board] substrate.

33. (Amended) A method of attaching at least two semiconductor die to a substrate, comprising:

providing at least two semiconductor die, each semiconductor die having a surface having at least one bond pad thereon;

providing a substrate having a die side surface, a second attachment surface, at least two vias extending through the [board] substrate from the die side surface to the second attachment surface, at least two circuits, and at least two bond pads located on the second attachment surface of the [board] substrate;

attaching the surface having at least one bond pad thereon of a semiconductor die of the at least two semiconductor die to the die side surface of the [board] substrate having the at least one bond pad of the semiconductor die located over one of the at least two vias extending through the [board] substrate ; and

connecting said at least one of each of the semiconductor die to said at least two bond pads of said [board] substrate using at least two wire bonds, at least one wire bond of said at least two wire bonds extending through the one via extending through the board of the at least two vias extending through the [board] substrate.

42. (Amended) A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace thereon;

providing a board having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the die side surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the die side surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pads of said board using at least one wire bond[, said at least one wire bond extending through the at least one via extending through then board]; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board.

45. (Amended) A method of attaching a plurality of semiconductor die to a master board, comprising:

providing a plurality of semiconductor die, each semiconductor die having at least one bond pad thereon;

providing a master board having a plurality of circuit traces thereon;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the die side surface of the board;

providing a plurality of electrical connectors for connecting [the] a plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching each semiconductor die of the plurality of semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of each semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds[, at least one wire bond of said plurality of wire

bonds extending through at least one via of the plurality of vias extending through then board]; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board.